WHAT IS CLAIMED IS:

1. A method of forming a conductive structure within an integrated circuit comprising:

forming a conformal tungsten layer over a dielectric layer and within openings within the dielectric layer;

forming a protective barrier layer over the tungsten layer, wherein the protective barrier layer comprises a material for which removal by chemical mechanical polishing is primarily mechanical; and

removing at least portions of the protective barrier layer and the tungsten layer by chemical mechanical polishing.

2. The method as set forth in Claim 1 wherein the step of forming a protective barrier layer over the tungsten layer further comprises:

forming a titanium or titanium nitride layer on the tungsten layer.

3. The method as set forth in Claim 2 wherein the step of removing at least portions of the protective barrier layer and the tungsten layer by chemical mechanical polishing further comprises:

removing portions of the tungsten layer overlying the dielectric layer without removing portions of the tungsten layer within the openings within the dielectric layer.

4. The method as set forth in Claim 3 wherein the step of removing at least portions of the protective barrier layer and the tungsten layer by chemical mechanical polishing further comprises:

removing all of the protective barrier layer.

5. The method as set forth in Claim 3 wherein the step of removing at least portions of the protective barrier layer and the tungsten layer by chemical mechanical polishing further comprises:

removing portions of the protective barrier layer overlying dielectric regions between the openings within the dielectric layer.

6. The method as set forth in Claim 5 wherein the step of removing at least portions of the protective barrier layer and the tungsten layer by chemical mechanical polishing further comprises:

after removing portions of the protective barrier layer overlying the dielectric regions between the openings within the dielectric layer, removing portions of the tungsten layer overlying the dielectric regions between the openings within the dielectric layer; and

during removal of portions of the tungsten layer overlying the dielectric regions between the openings within the dielectric layer, removing portions of the protective barrier layer overlying the openings within the dielectric layer.

7. The method as set forth in Claim 2 wherein the step of removing at least portions of the protective barrier layer and the tungsten layer by chemical mechanical polishing further comprises:

removing portions of the protective barrier layer and the tungsten layer overlying dielectric regions between the openings within the dielectric layer to planarize remaining portions of the tungsten layer and remaining portions of the protective barrier layer, if any, with the dielectric layer.

8. A portion of an integrated circuit structure comprising:

a dielectric layer over a substrate;

a conformal tungsten layer over the dielectric layer and within openings within the dielectric layer; and

a protective barrier layer over the tungsten layer, wherein the protective barrier layer comprises a material for which removal by chemical mechanical polishing is primarily mechanical.

9. The portion of an integrated circuit structure as set forth in Claim 8 wherein the protective barrier layer is titanium or titanium nitride.

10. The portion of an integrated circuit structure as set forth in Claim 8 wherein portions of the tungsten layer within the openings are thicker than portions of the tungsten layer over the dielectric layer.

11. The portion of an integrated circuit structure as set forth in Claim 8 wherein the protective barrier layer overlies the entire tungsten layer.

12. The portion of an integrated circuit structure as set forth in Claim 8 wherein the protective barrier layer overlies portions of the tungsten layer within the openings but not portions of the tungsten layer over the dielectric layer.

13. The portion of an integrated circuit structure as set forth in Claim 8 wherein the tungsten layer has a thickness of between about 4500 and 8000 angstroms.

14. The portion of an integrated circuit structure as set forth in Claim 8 wherein the protective barrier layer has a thickness of between about 100 and 800 angstroms.

15. The portion of an integrated circuit structure as set forth in Claim 8 wherein at least one opening within the dielectric layer is sized to form a capacitive electrode from tungsten within the at least one opening.

16. A portion of an integrated circuit structure comprising:

a dielectric layer having an opening therein;

tungsten within the opening; and

a portion of a protective barrier layer over a central region of the tungsten within the opening.

17. The portion of an integrated circuit structure as set forth in Claim 16 wherein the portion of the protective barrier layer comprises a material for which removal by chemical mechanical polishing is primarily mechanical.

18. The portion of an integrated circuit structure as set forth in Claim 16 wherein the portion of the protective barrier layer is titanium or titanium nitride.

19. The portion of an integrated circuit structure as set forth in Claim 16 wherein the tungsten and the portion of the protective barrier layer form an upper surface which is substantially planar with an upper surface of the dielectric layer.

20. The portion of an integrated circuit structure as set forth in Claim 16 wherein the opening within the dielectric layer is sized to form a capacitive electrode from the tungsten within the opening.